**WHAT IS CLAIMED IS:**

1. A multi-mode voltage-controlled oscillator (VCO) comprising:

a ring oscillator circuit comprising a series connection of an odd number K of logic inverter gates, wherein K is greater than three;

a forward conduction circuit having a first input, a first output, and receiving control inputs, said forward conduction circuit coupled in parallel with a selected sequence of logic inverter gates within said K logic inverter gates; and

a selectable inverter circuit, having a first inverter input, a first inverter output and receiving a first mode control signal and a second mode control signal, said first inverter input coupled to a logic input of an Nth logic inverter gate and said first inverter output coupled to a logic output of said Nth logic inverter gate, said Nth logic inverter gate selected from said K logic inverter gates, wherein a frequency range of said multi-mode VCO is selected in response to states of said first and second mode control signals.

2. The multi-mode VCO of claim 1, wherein said selectable inverter circuit comprises:

a selectable logic inverter gate having an input coupled to said first inverter input, an output coupled to said first inverter output, a first terminal for receiving a first power supply voltage, and a second terminal for receiving a second power supply voltage;

a first electronic switch having a first control input receiving said first mode control signal, a first switch terminal receiving said first power supply voltage, and a second switch terminal coupled to said first terminal of said selectable inverter; and

a second electronic switch having a second control input receiving said second mode signal, a third switch terminal receiving said second power supply voltage, and a fourth switch terminal coupled to said second terminal of said selectable inverter.

3. The multi-mode VCO of claim 1, wherein said forward conduction circuit comprises:

a control inverter having a second input and a second output; and

a bi-directional conduction circuit having a third input, a third output, a first control input, and a second control input, said second input coupled to said first input, said second output coupled to said third input, said third output coupled to said first output, said first control input coupled to a first control voltage, and said second control input coupled to a second control voltage.

4. The multi-mode VCO of claim 3, wherein said bi-directional conduction circuit comprises:

a first P channel metal oxide semiconductor (PFET) having a first drain terminal, a first source terminal and a first gate terminal; and

a first NFET having a second drain terminal, a second source terminal and a second gate terminal, wherein said first drain terminal and said second drain terminal are coupled to said third input, said first source terminal and said second source terminal are coupled to said third output, said first gate terminal is coupled to said first control input, and said second gate terminal is coupled to said second control input.

5. The multi-mode VCO of claim 2, wherein said first electronic switch comprises a third PFET having a fifth drain terminal, a fifth source terminal and a fifth gate terminal, said fifth source terminal coupled to said first electronic switch terminal, said fifth drain terminal coupled to said second electronic switch terminal, and said fifth gate terminal coupled to said first control input.

6. The multi-mode VCO of claim 2, wherein said second electronic switch comprises a third NFET having a sixth drain terminal, a sixth source terminal and a sixth gate terminal, said sixth source terminal coupled to said third electronic switch terminal, said sixth drain terminal coupled to said fourth electronic switch terminal, and said sixth gate terminal coupled to said second control input.

7. The multi-mode VCO of claim 1, wherein said selected sequence from said K logic inverter gates comprises a series of three inverter logic gates.

8. The multi-mode VCO of claim 1, wherein each of said K inverter logic gates of said ring oscillator are coupled in parallel with a corresponding one of said selectable inverter circuits.

9. A data processing system comprising:

a central processor unit (CPU), operable to generate a clock signal with a phase lock loop (PLL) clock generator, having a ring oscillator circuit configured as a series connection of an odd number K of logic inverter gates, wherein K is greater than three, a forward conduction circuit having a first input, a first output, and receiving control inputs, said forward conduction circuit coupled in parallel with a selected sequence from said K logic inverter gates, and a selectable inverter circuit, having a first inverter input, a first inverter output and receiving a first mode control signal and a second mode control signal, said first inverter input coupled to a logic input of an Nth logic inverter gate and said first inverter output coupled to a logic output of said Nth logic inverter gate, said Nth logic inverter gate selected from said K logic inverter gates;

a random access memory (RAM);

a read only memory (ROM);

an I/O adapter; and

a bus system coupling said CPU to said ROM,, said I/O adapter, and said RAM, wherein a frequency range of said ring oscillator circuit is selected in response to states of said first and second mode control signals.

10. The data processing system of claim 9, wherein said selectable inverter circuit comprises:

a selectable logic inverter gate having an input coupled to said first inverter input, an output coupled to said first inverter output, a first terminal for receiving a first power supply voltage, and a second terminal for receiving a second power supply voltage;

a first electronic switch having a first control input receiving said first mode control signal, a first switch terminal receiving said first power supply voltage, and a

second switch terminal coupled to said first terminal of said selectable inverter; and

a second electronic switch having a second control input receiving said second mode signal, a third switch terminal receiving said second power supply voltage, and a fourth switch terminal coupled to said second terminal of said selectable inverter.

11. The data processing system of claim 9, wherein said forward conduction circuit comprises:

a control inverter having a second input and a second output; and

a bi-directional conduction circuit having a third input, a third output, a first control input, and a second control input, said second input coupled to said first input, said second output coupled to said third input, said third output coupled to said first output, said first control input coupled to a first control voltage, and said second control input coupled to a second control voltage.

12. The data processing system of claim 11, wherein said bi-directional conduction circuit comprises:

a first P channel metal oxide semiconductor (PFET) having a first drain terminal, a first source terminal and a first gate terminal; and

a first NFET having a second drain terminal, a second source terminal and a second gate terminal, wherein said first drain terminal and said second drain terminal are coupled to said third input, said first source terminal and said second source terminal are coupled to said third output, said first gate terminal is coupled to said first control input, and said second gate terminal is coupled to said second control input.

13. The data processing system of claim 10, wherein said first electronic switch comprises a third PFET having a fifth drain terminal, a fifth source terminal and a fifth

gate terminal, said fifth source terminal coupled to said first electronic switch terminal, said fifth drain terminal coupled to said second electronic switch terminal, and said fifth gate terminal coupled to said first control input.

14. The data processing system of claim 10, wherein said second electronic switch comprises a third NFET having a sixth drain terminal, a sixth source terminal and a sixth gate terminal, said sixth source terminal coupled to said third electronic switch terminal, said sixth drain terminal coupled to said fourth electronic switch terminal, and said sixth gate terminal coupled to said second control input.

15. The data processing system of claim 9, wherein said selected sequence from said K logic inverter gates comprises a series of three inverter logic gates.

16. The data processing system of claim 9, wherein each of said K inverter logic gates of said ring oscillator are coupled in parallel with a corresponding one of said selectable inverter circuits.

17. A phase lock loop (PLL) circuit comprising:

a phase/frequency comparator receiving a reference clock signal and a feedback clock signal and generating a first control signal and a second control signal;

a charge pump circuit receiving said first control signal and said second control signal and generating a charge pump output on a first and second charge pump nodes;

a first capacitor and a second capacitor coupled to said first and said second charge pump nodes, respectively;

a voltage controlled oscillator (VCO) having a ring oscillator circuit having a series connection of an odd number K of logic inverter gates, wherein K is greater than three;

a forward conduction circuit having a first input, a first output, and receiving said charge pump output, said forward conduction circuit coupled in parallel with a selected sequence of logic inverter gates within said K logic inverter gates, and a selectable inverter circuit, having a first inverter input, a first inverter output and receiving a first mode control signal and a second mode control signal, said first inverter input coupled to a logic input of an Nth logic inverter gate and said first inverter output coupled to a logic output of said Nth logic inverter gate, said Nth logic inverter gate selected from said K logic inverter gates, wherein a frequency range of said VCO is selected in response to states of said first and second mode control signals; and

a signal frequency divider receiving said VCO output signal and generating said feedback clock signal, wherein a frequency of said VCO is controlled in response to said charge pump output and said first and second mode control signals.

18. The PLL circuit of claim 19, wherein said selectable inverter circuit comprises:

a selectable logic inverter gate having an input coupled to said first inverter input,

an output coupled to said first inverter output, a first terminal for receiving a first power supply voltage, and a second terminal for receiving a second power supply voltage;

a first electronic switch having a first control input receiving said first mode control signal, a first switch terminal receiving said first power supply voltage, and a second switch terminal coupled to said first terminal of said selectable inverter; and

a second electronic switch having a second control input receiving said second mode signal, a third switch terminal receiving said second power supply voltage, and a fourth switch terminal coupled to said second terminal of said selectable inverter.

19. The PLL circuit of claim 19, wherein said forward conduction circuit comprises:

a control inverter having a second input and a second output; and

a bi-directional conduction circuit having a third input, a third output, a first control input, and a second control input, said second input coupled to said first input, said second output coupled to said third input, said third output coupled to said first output, said first control input coupled to a first control voltage, and said second control input coupled to a second control voltage.

20. The PLL circuit of claim 21, wherein said bi-directional conduction circuit comprises:

a first P channel metal oxide semiconductor (PFET) having a first drain terminal, a first source terminal and a first gate terminal; and

a first NFET having a second drain terminal, a second source terminal and a second gate terminal, wherein said first drain terminal and said second drain terminal are coupled to said third input, said first source terminal and said second source terminal are coupled to said third output, said first gate terminal is coupled to said first control input, and said second gate terminal is coupled to said second control input.

21. The PLL circuit of claim 20, wherein said first electronic switch comprises a third PFET having a fifth drain terminal, a fifth source terminal and a fifth gate terminal, said fifth source terminal coupled to said first electronic switch terminal, said fifth drain terminal coupled to said second electronic switch terminal, and said fifth gate terminal coupled to said first control input.

22. The PLL circuit of claim 20, wherein said second electronic switch comprises a third NFET having a sixth drain terminal, a sixth source terminal and a sixth gate terminal, said sixth source terminal coupled to said third electronic switch terminal, said sixth drain terminal coupled to said fourth electronic switch terminal, and said sixth gate terminal coupled to said second control input.

23. The PLL circuit of claim 19, wherein said selected sequence from said K logic inverter gates comprises a series of three inverter logic gates.

24. The PLL circuit of claim 19, wherein each of said K inverter logic gates of said ring oscillator are coupled in parallel with a corresponding one of said selectable inverter circuits.